**Version with Markings to Show the Changes Made**

**In the Claims:**

Claims 26, 28, 30, 36, and 39 have been amended as follows:

26. (Twice amended) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate;

a stack of metal layers alternating with dielectric layers on the substrate, wherein the metal layers are coupled with one another by a plurality of via plugs in the dielectric layers, the via plugs being placed in alternating manner with respect to one another through the stack, and the metal layers are in a concentric circle arrangement, to reduce the capacitance by reducing the area of the substrate overlapped by the metal layers;

an uppermost metal layer positioned on the stack and electrically connected to the stack, wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer; and

a passivation layer having a bonding pad opening positioned on the uppermost metal layer for externally electric connection.

28. (Twice amended) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate;

a stack of metal layers alternating with dielectric layers on the substrate, wherein the metal layers are coupled with one another by a plurality of via plugs through the dielectric layers and are placed in a concentric circle arrangement, to reduce the capacitance by reducing the area of the substrate overlapped by the metal layers;

an uppermost metal layer positioned on the stack and electrically connected to the stack; and

a passivation layer having a bonding pad opening on the uppermost metal layer for externally electric connection.

30. (Twice Amended) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region; and

a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by a plurality of via plugs through the dielectric layers, wherein the bonding pad [being] is aligned with the doped region and the metal layers are in a concentric circle arrangement to reduce the capacitance by reducing the area of the substrate overlapped by the metal layers.

36. (Once Amended) A semiconductor device, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region;

a bonding pad on the substrate, the bonding pad being comprising a stack of metal lyers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by a plurality of via plugs through the dielectric layers, wherein the bonding pad is aligned with the doped region, and wherein the metal layers in the stack are in a concentric circle arrangement to reduce the area of the substrate overlapped by the metal layers; and

a semiconductor device under the bonding pad.

39. (Once Amended) A semiconductor device, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region;

a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by means of a plurality of via plugs, wherein the bonding pad is aligned with the doped region; and wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer, and the metal layers are in a concentric circle arrangement to reduce the area of the substrate overlapped by the metal layers;

and

a semiconductor device under the bonding pad.

Cancel claims 27, 33, and 40.